

Capacitive Voltage Transformers: Transient Overreach Concerns and Solutions for Distance Relaying

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CAPACITIVE VOLTAGE TRANSFORMERS: TRANSIENT OVERREACH CONCERNS AND SOLUTIONS FOR DISTANCE RELAYING

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ABSTRACT

Capacitive Voltage Transformers (CVTs) are common in high-voltage transmission line applications. These same applications require fast, yet secure protection. However, as the requirement for faster protective relays grows, so does the concern over the poor transient response of some CVTs for certain system conditions.

Solid-state and microprocessor relays can respond to a CVT transient due to their high operating speed and increased sensitivity. This paper discusses CVT models whose purpose is to identify which major CVT components contribute to the CVT transient. Some surprises include a recommendation for CVT burden and the type of ferroresonant-suppression circuit that gives the least CVT transient.

This paper also reviews how the System Impedance Ratio (SIR) affects the CVT transient response. The higher the SIR, the worse the CVT transient for a given CVT.

Finally, this paper discusses improvements in relaying logic. The new method of detecting CVT transients is more precise than past detection methods and does not penalize distance protection speed for close-in faults.

INTRODUCTION

Poor CVT transient response and the distance element overreach it causes are a serious concern for high-speed line protection.

For faults that cause very depressed phase voltages, the CVT output voltage may not closely follow its input voltage due to the internal CVT energy storage elements. Because these elements take time to change their stored energy, they introduce a transient to the CVT output following a significant input voltage change. In this paper, we define the duration of CVT transient as that time period during which the CVT output voltage does not match the ratio input voltage.

CVT transients reduce the fundamental component of the fault voltage. This decrease in the fundamental voltage component results in a decrease in the calculated impedance. If the fundamental voltage reduction is great enough, Zone 1 distance elements undesirably pick up for out-of-section faults.

If a fault is within that portion of line protected by a Zone 1 element, the resulting distance calculation decrease due to a CVT transient is tolerable; the protective relay should operate. However, if the fault is located outside of that portion of line protected by the Zone 1 element and the CVT transient causes the Zone 1 element to pick up, then this CVT transient is not tolerable.

One solution to the CVT-transient-induced distance element overreach problem for out-of-section faults has been to reduce the Zone 1 element reach. However, the CVT transient response for some applications requires such a reduction of the Zone 1 distance element reach that the Zone 1 element is no longer effective protection. Another solution is to delay all Zone 1 distance element operations. This delay prevents the distance element from producing a trip output during the CVT transient. The later solution is undesirable in that close-in fault clearance times are penalized unnecessarily.

This paper addresses the following questions:

- What is the structure of a CVT, and how can we determine its transient response?

The first section of the paper describes the components that make up CVTs. This section discusses how some key CVT components, such as coupling capacitors and ferroresonance-suppression circuits, relate to the CVT transient performance.

- How do CVT transients and other system parameters affect the performance of distance relaying?

The second section of the paper discusses CVT and relay models. We use these models to study the performance of distance relays during CVT transients, under different SIRs, and for a variety of CVT loading conditions.

- What are the possible solutions to the distance element overreach problem?

The last section compares different techniques of solving the distance element overreach problem due to CVT transients and proposes a new method.

CAPACITIVE VOLTAGE TRANSFORMER COMPONENTS

A CVT (Figure 1) consists of the following components:

- Coupling capacitors (C_1 and C_2)
- Compensating reactor (L)
- Step-down transformer
- Ferroresonance-suppression circuit

When equipped with a communication carrier, the CVT has an additional drain coil, choke coil, and carrier switch that are not shown in Figure 1.

The coupling capacitors of the CVT function as a voltage divider to step down the line voltage to an intermediate-level voltage, typically 5 to 15 kV. The compensating reactor cancels the coupling capacitor reactance at the system frequency. This reactance cancellation prevents any phase shift between the primary and secondary voltages at the system frequency. The step-down transformer further reduces the intermediate-level voltage to the nominal relaying voltage, typically $115/\sqrt{3}$ volts.

The compensating reactor and step-down transformer have iron cores. Besides introducing copper and core losses, the compensating reactor and step-down transformer also produce ferroresonance due to the nonlinearity of the iron cores. CVT manufacturers recognize this ferroresonance phenomenon and include a ferroresonance-suppression circuit. This circuit is normally used on the secondary of the step-down transformer. While this circuit is required to avoid dangerous and destructive overvoltages caused by ferroresonance, it can aggravate the CVT

transient. Whether or not this suppression circuit aggravates the CVT transient depends upon the suppression circuit design. We discuss suppression circuits later in the paper.

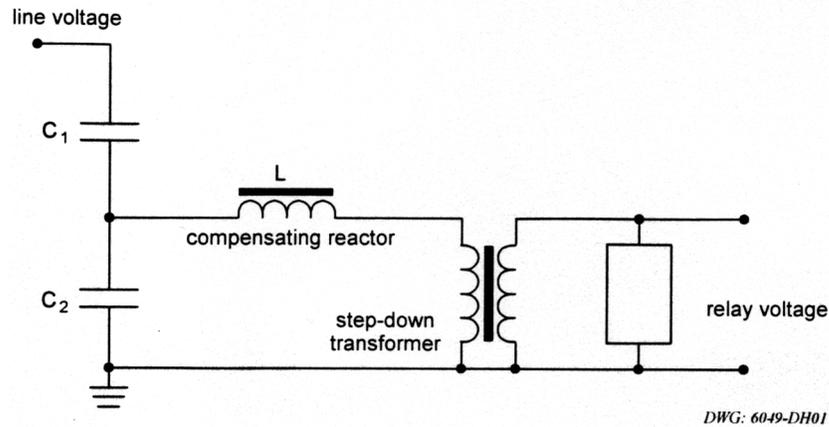


Figure 1 Generic CVT Structure

When a fault suddenly reduces the line voltage, the CVT secondary output does not instantaneously represent the primary voltage. This is because the energy storage elements, such as coupling capacitors and the compensating reactor, cannot instantaneously change their charge or flux. These energy storage elements cause the CVT transient.

CVT transients differ depending on the fault point-on-wave (POW) initiation. The CVT transients for faults occurring at voltage peaks and voltage zeros are quite distinctive and different. Figure 2 and Figure 3 show two CVT transients for zero-crossing and peak POW fault initiations. For comparison, the ideal CVT voltage output (ratio voltage) is shown in each figure. Figure 2 shows a CVT transient with a fault occurring at a voltage zero. Also, notice that the CVT output does not follow the ideal output until 1.75 cycles after fault inception.

Figure 3 shows the CVT response to the same fault occurring at a voltage peak. Again, the CVT output does not follow the ideal output. The CVT transient for this case lasts about 1.25 cycles. The CVT transient response to a fault occurring at points other than a voltage peak or voltage zero take a wave shape in between those shown in Figure 2 and Figure 3.

Each CVT component contributes to the CVT transient response. For example, the turns ratio of the step-down transformer dictates how well a CVT isolates its burden from the dividing capacitors C_1 and C_2 . The higher the transformer ratio, the less effect the CVT burden has on these capacitors. The different loading on the CVT coupling capacitors due to different transformer ratios changes the shape and duration of CVT transients.

Next, we discuss how two key CVT components affect the CVT transient response: the coupling capacitors and ferroresonance-suppression circuit.

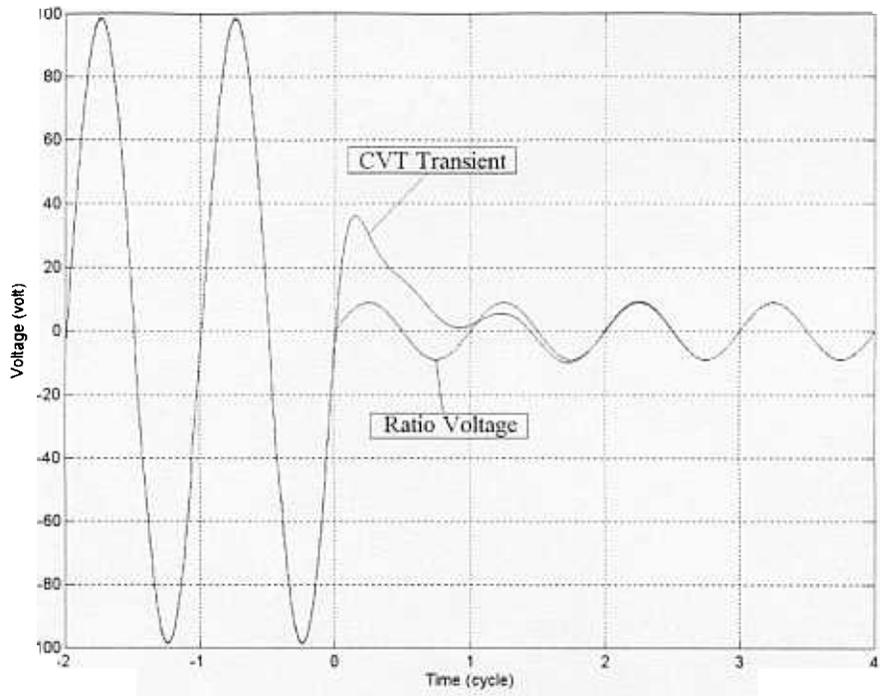


Figure 2 CVT Transient with Fault at Voltage Zero

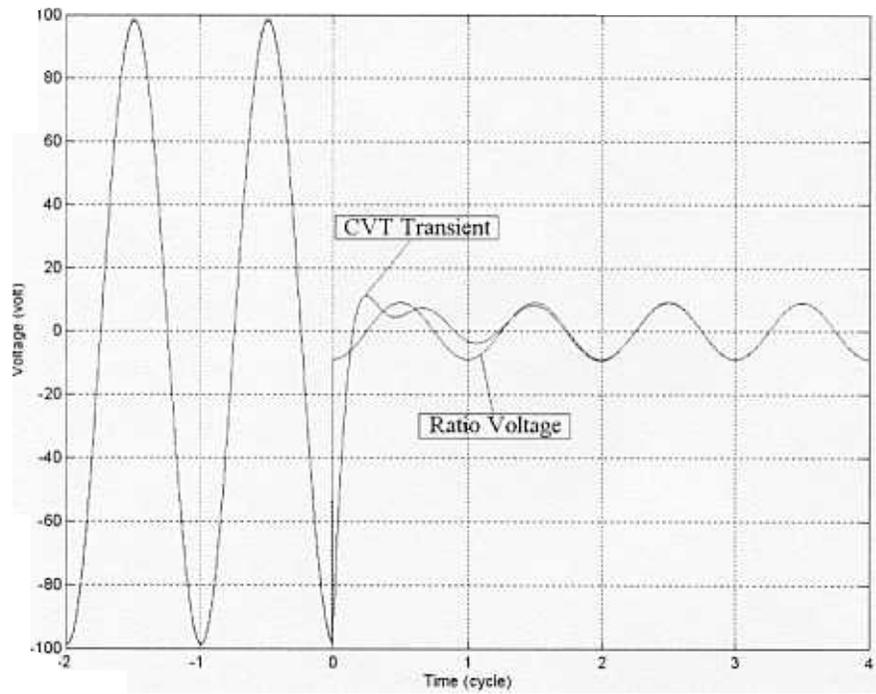


Figure 3 CVT Transient with Fault at Voltage Peak

Coupling Capacitor Value Affects CVT Transient Response

A CVT is made up of a number of capacitor units connected in series. The number of capacitor units depends on the applied primary voltage level. The CVT capacitance is represented by two values: one for the equivalent capacitance above the intermediate voltage point (C_1) and the other for the equivalent capacitance below the intermediate voltage point (C_2). The Thevenin equivalent capacitance value ($C_1 + C_2$) is different from the total capacitance $C_1 \cdot C_2 / (C_1 + C_2)$ normally given by CVT manufacturers. $C_1 + C_2$ is approximately 100 nano-farad (nF) for the CVTs studied in this paper. Some CVT manufacturers differentiate CVTs as normal-, high-, or extra high-capacitance CVTs.

The high capacitance value in a CVT decreases the CVT transient in magnitude. See this by comparing the CVT transient plots of Figure 2 and Figure 4 for a fault initiated at a voltage zero. Figure 4 shows the transient response of a CVT with four times total capacitance of that shown in Figure 2.

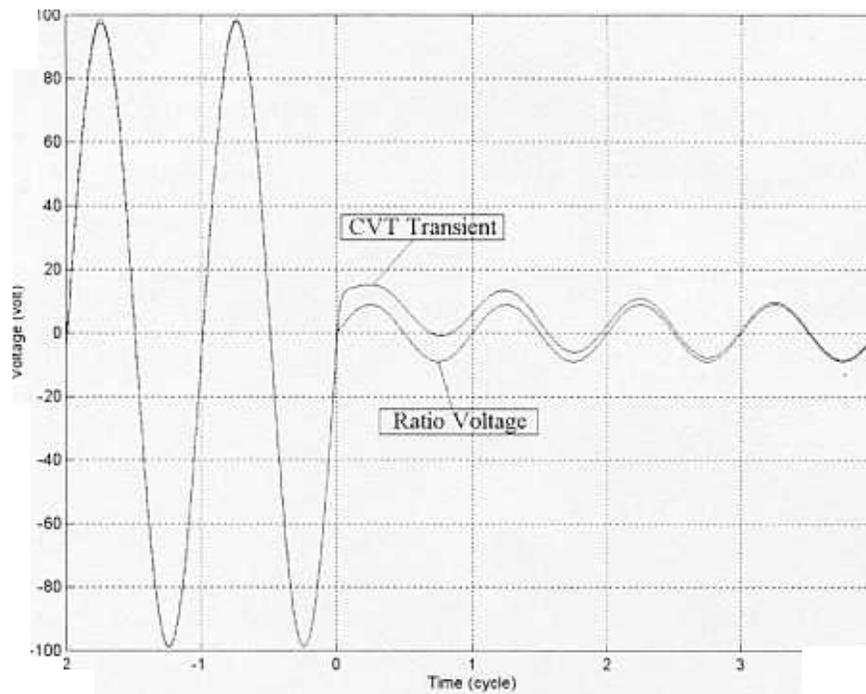


Figure 4 Transient Response of a High-Capacitance CVT

Distance elements calculate a fault apparent impedance based on the fundamental components of the fault voltage and current. The fundamental content of the CVT transient determines the degree of distance element overreach. Figure 5 shows the fundamental components of the same CVT outputs shown in Figure 2 and Figure 4. We obtained the fundamental magnitudes by filtering the CVT outputs using a digital band-pass filter. Notice that the fundamental component of the higher capacitance CVT output voltage is closer to the true fundamental magnitude than that of the lower capacitance CVT. Therefore, any distance element overreach caused by a transient output of a higher capacitance CVT is much smaller than that caused by the transient output of a lower capacitance CVT.

Increasing the CVT capacitance value can increase the CVT cost but decreases the CVT transient response. Thus, protection engineers must strike a balance between CVT performance and CVT cost.

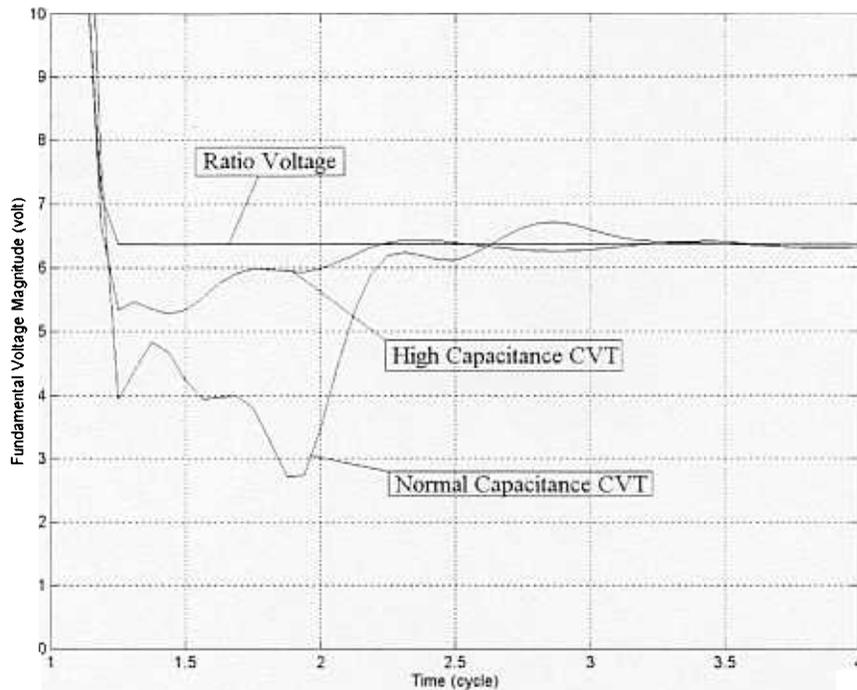
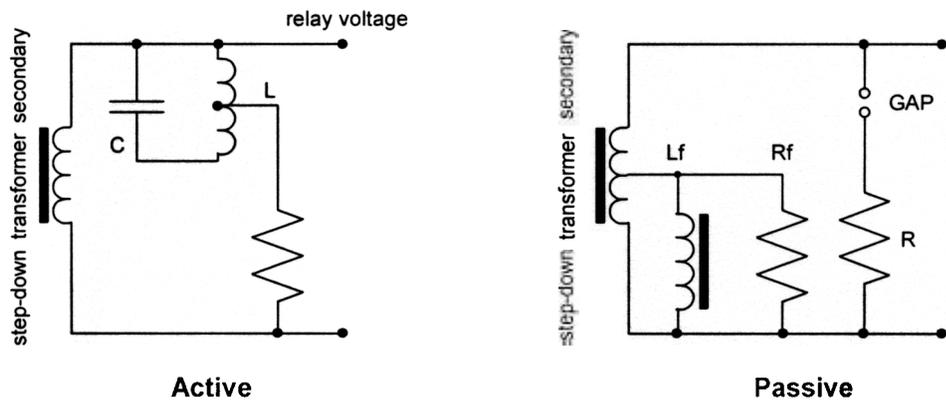


Figure 5 Higher Capacitance CVT Causes Less Reduction in the Fundamental Voltage Magnitude

Ferroresonance-Suppression Circuit Design Affects CVT Transient Response

Figure 6 shows two types of ferroresonance-suppression circuits.



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Figure 6 Active and Passive Ferroresonance-Suppression Circuits

Active Ferroresonance-Suppression Circuits

Active ferroresonance-suppression circuits (AFSC) consist of an LC parallel tuning circuit with a loading resistor. The LC tuning circuit resonates at the system frequency and presents a high impedance to the fundamental voltage. The loading resistor is connected to a middle tap of the inductor to increase the resonant impedance of the circuit. For frequencies above or below the fundamental frequency (off-nominal frequencies), the LC parallel resonant impedance gradually

reduces to the resistance of the loading resistor and attenuates the energy of off-nominal-frequency voltages.

Passive Ferroresonance-Suppression Circuits

Passive ferroresonance-suppression circuits (PFSC) have a permanently connected loading resistor R_f , a saturable inductor L_f , and an air-gap loading resistor R . Under normal operating conditions, the secondary voltage is not high enough to flash over the air gap, and the loading resistor R has no effect on the CVT performance. Once a ferroresonance oscillation exists, the induced voltage flashes over the gap and shunts in the loading resistance to attenuate the oscillation energy. L_f is designed to saturate at about 150% of nominal voltage to further prevent a sustained ferroresonance condition.

Ferroresonance-Suppression Circuit Effects on CVT Transient Performance

The AFSC acts like a band-pass filter and introduces extra time delay in the CVT secondary output. The energy storage elements in the AFSC contribute to the severity of the CVT transient.

In contrast, the PFSC has little effect on the CVT transient. The majority components of the circuit are isolated from the CVT output when ferroresonance is not present. Figure 7 shows the difference of the CVT secondary outputs for a CVT with an AFSC and a CVT with a PFSC for the same fault voltage. Note that the CVT with a PFSC has a better, less distorted transient response than the CVT with an AFSC. This less distorted transient results in a fundamental magnitude that is closer to the true fundamental magnitude as shown in Figure 8.

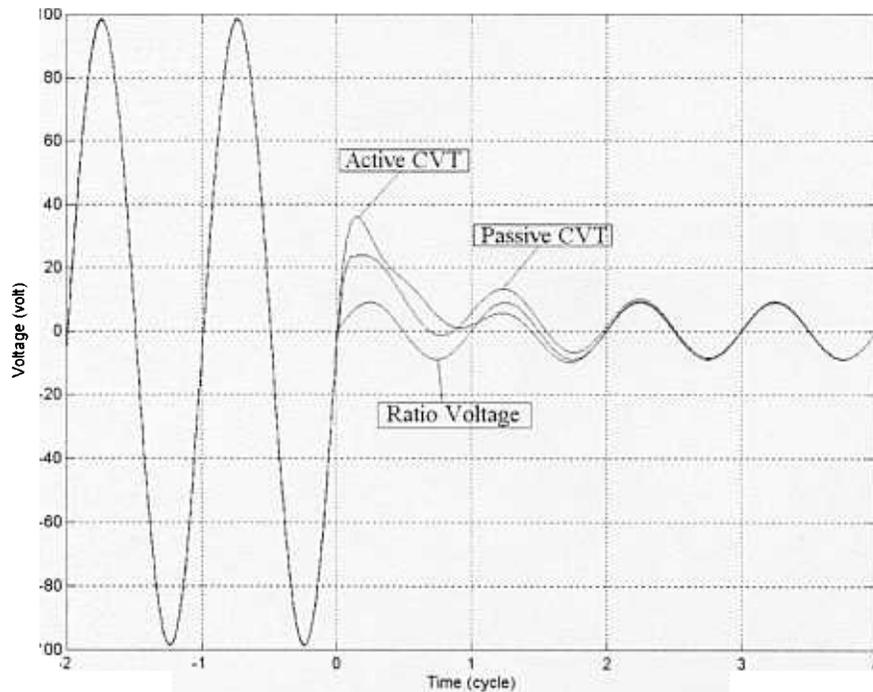


Figure 7 CVT Transients of AFSC and PFSC

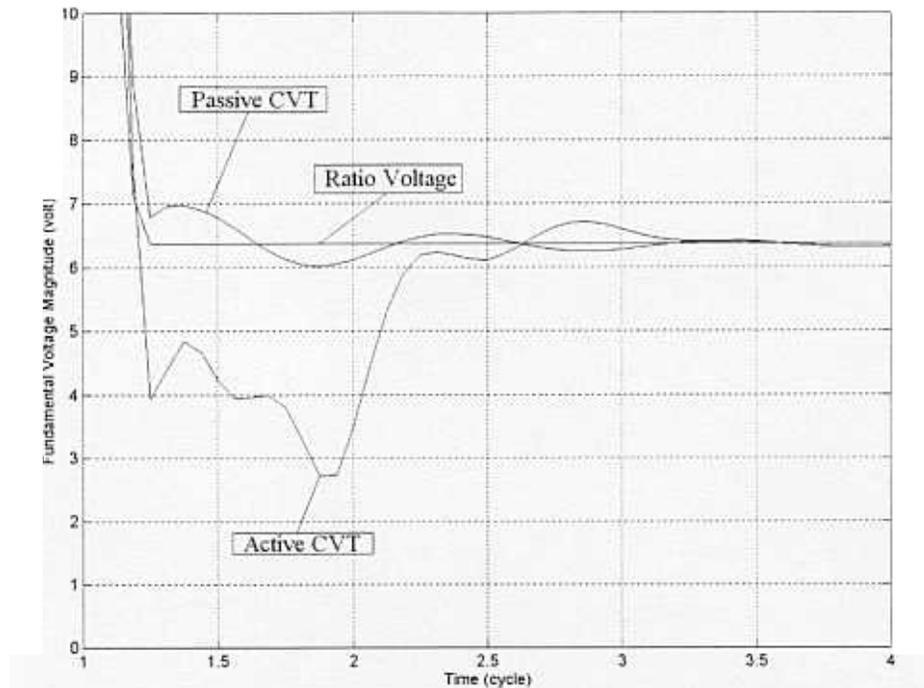
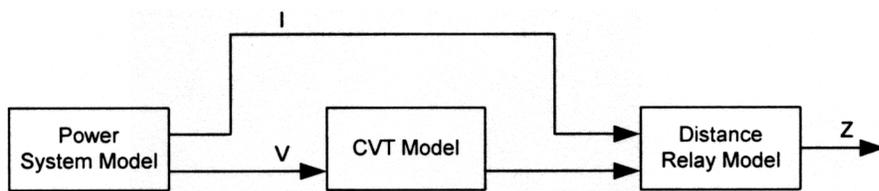


Figure 8 CVT with PFSC Causes Less Fundamental Component Reduction

The PFSC has a permanently connected resistor, which increases the VA loading of the intermediate step-down transformer. For the same burden specification, the CVT with PFSC requires a bigger intermediate step-down transformer.

DISTANCE RELAY PERFORMANCE

We modeled a simple power system, CVTs with AFSC and PFSC, and a generic distance relay to determine the performance of distance relays during CVT transients. The evaluation system is shown in Figure 9.

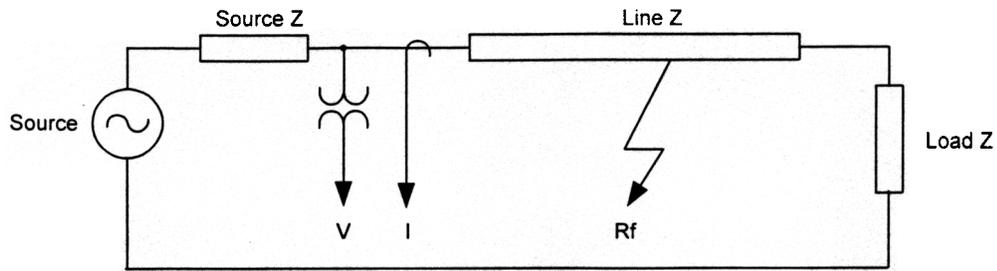


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Figure 9 Distance Relay Evaluation System

Power-System Model

Figure 10 shows the simple power-system model. It is a single phase, radial system with fixed line impedance and variable source impedance. The difference between pre-fault and fault voltage levels heavily affects the CVT transient magnitude and duration. This voltage difference is determined by SIR values, fault locations, and fault resistance (R_f).



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Figure 10 Power-System Model

CVT Model

We used linear models for an active and a passive CVT. The parameters used in the models are from Reference [1]. The model includes the following CVT components:

- Coupling capacitors
- Compensating inductor
- Step-down transformer
- Ferroresonance-suppression circuit
- Burden

The stray capacitance and copper resistance of the compensating reactor and step-down transformer are included in the model to improve its accuracy at high frequencies.

All CVT model frequency responses were verified against those obtained from [1]. We also compared the CVT transient outputs at voltage peaks and voltage zeros and verified them as being the same as those shown in [2].

The top plot in Figure 11 shows the frequency response of a CVT with an AFSC. Ideally, the frequency response should be a flat line at 0 dB, which means the CVT passes all frequency components without attenuation. Passing all frequency components makes the CVT output voltage a close representation of its input voltage. If the frequency response shows attenuation at different frequencies, the CVT then behaves much like a filter and introduces transients and time delay.

The bottom plot of Figure 11 is the CVT output together with the ratio voltage. Ideally, we would like to see that the CVT output voltage is close to the ratio voltage. However, notice that the CVT output voltage does not match the ratio voltage for 1.75 cycles.

Figure 12 shows the frequency response of the CVT with a PFSC. Notice that this frequency response is much flatter than the one shown in Figure 11. All CVT parameters used in this paper and the system and fault configurations are listed in the Appendix.

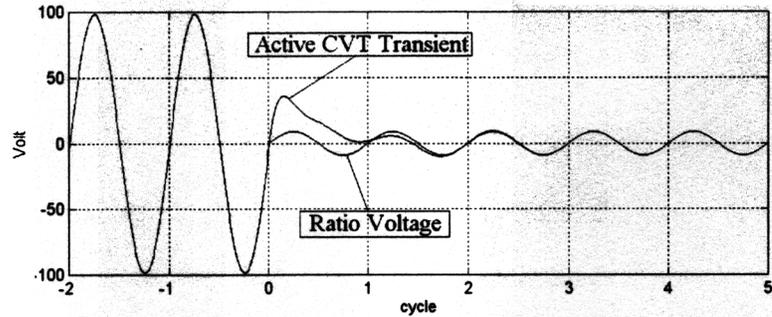
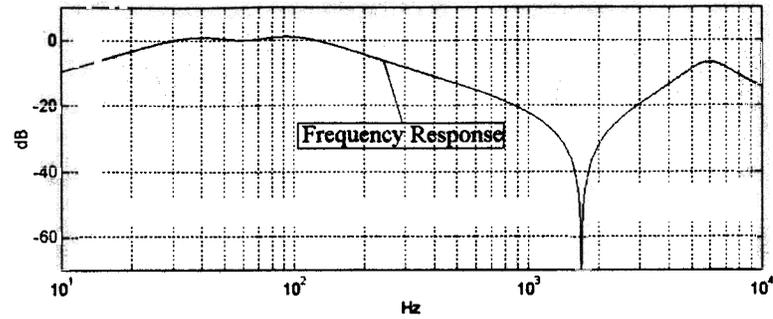


Figure 11 Active CVT Model Result

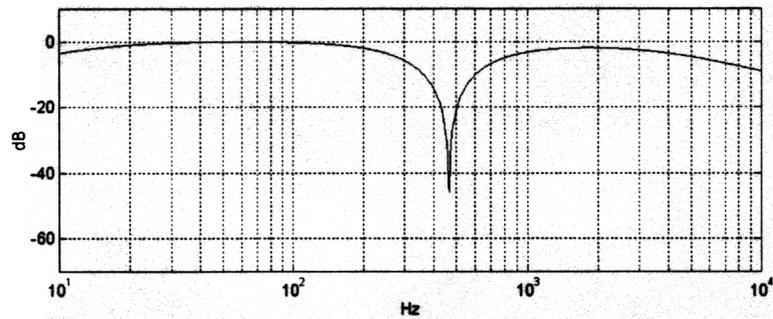
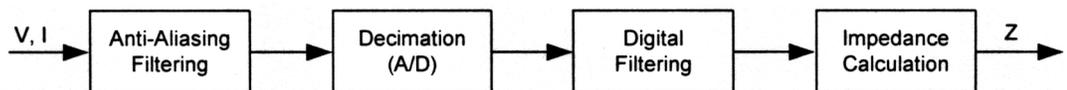


Figure 12 Frequency Response of Passive CVT Model

Relay Model

Figure 13 shows the distance relay model we used to evaluate the CVT transient effects. This model includes an analog anti-aliasing low-pass filtering, analog-to-digital conversion (decimation), digital band-pass filtering, and impedance calculation. The generic distance relay does not include security measures or other means of preventing CVT-transient-induced overreach.



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Figure 13 The Relay Model

Distance Relay Performance

Figure 14 shows the generic distance relay response to the transients of CVTs with PFSC and AFSC. The fault applied is at the end of the radial line. The curves in the plot show the maximum Zone 1 reach setting so as not to pick up due to CVT transient errors.

From these curves, we see that the distance relay transient response for a CVT with a PFSC is much better because the relay has much less overreach. When using a CVT with a PFSC, the need to reduce the Zone 1 distance element reach is greatly reduced as compared to that required when using a CVT with an AFSC.

We limited fault POW initiations to voltage peaks and voltage zeros. The results shown in Figure 14 are the worst distance element overreach cases -- faults that occur at a voltage zero.

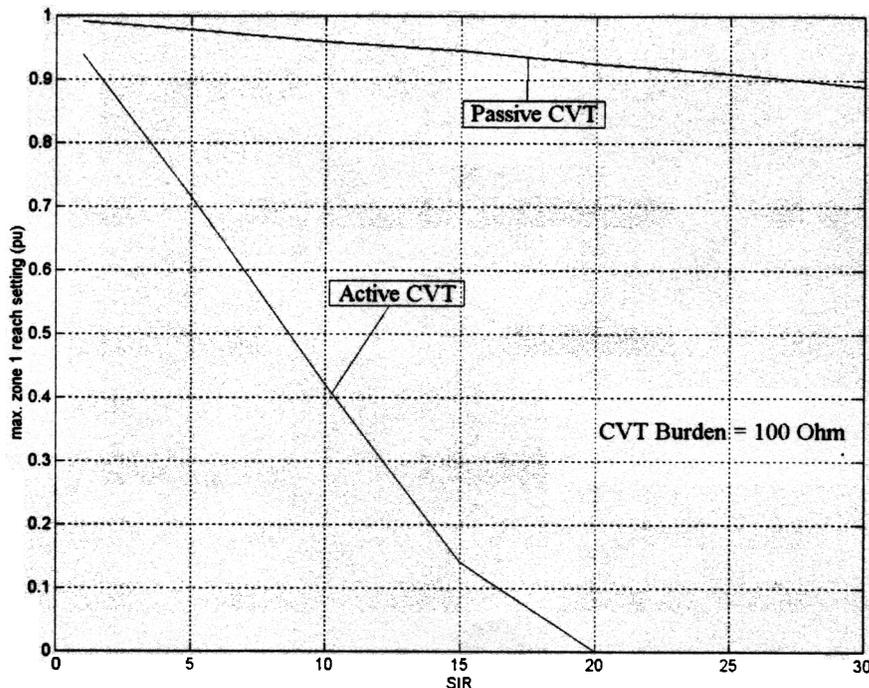


Figure 14 Distance Relay Performance with AFSC and PFSC

System Impedance Ratio (SIR)

The major factor that affects the severity of CVT transients is the fault voltage magnitude level. The smaller the fault voltage level, the greater the likelihood that the CVT will introduce a prolonged and distorted transient. SIR directly influences the fault voltage level for a fault at a given location. We must keep the SIR value in mind when assessing the influence of CVT transients on a distance relay.

Figure 14 shows a plot of maximum Zone 1 reach settings versus SIR values. When used with the CVT having an AFSC, the Zone 1 element of the generic distance relay can tolerate CVT transients for systems with SIRs up to four. Without any additional logic, the relay Zone 1 protection must be eliminated for systems with SIRs ≥ 20 .

The relay transient response when using a CVT with a PFSC is much better. The Zone 1 protection is effective for SIRs as high as 30.

CVT Burden

The CVT transient characteristic is influenced by the magnitude and angle of the connected burden.

ANSI C93.1-1990 standard [3] requires that the burden used for CVT transient response testing be two impedances connected in parallel as in Figure 15. One impedance is a resistance (R_p), and the other impedance, (R_s and X_s), has a lagging power factor of 0.5. The burden value is 100% or 25% of the CVT maximum rated accuracy class voltamperes and has a power factor of 0.85.

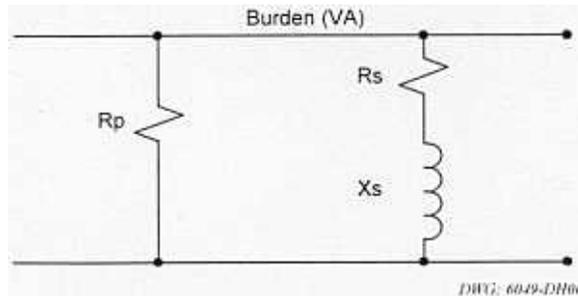


Figure 15 Burden for CVT Transient Testing

Figure 16 shows the maximum Zone 1 reach setting as a function of ANSI and resistive burdens for the CVT with a PFSC. The ANSI loading increases the CVT transient and distance element overreach as compared to the resistive burden.

Solid-state and microprocessor relays have very small and nearly resistive input burdens. When using a CVT, engineers need to calculate the total burden of all devices connected on the CVT and make sure the burden is not excessive and nearly resistive to assure proper distance relay protection.

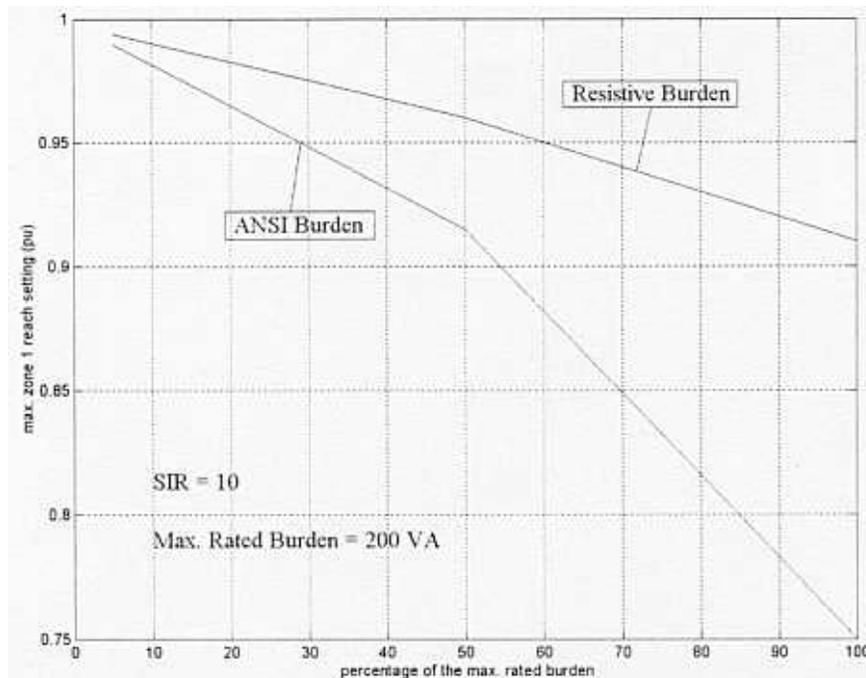


Figure 16 Relay Performance as a Function of CVT Burdens

CVT TRANSIENT DETECTION LOGIC

The generic distance relay has overreaching problems when:

- The system has a high SIR
- The CVT has an AFSC

This overreach problem is further aggravated if the CVT has a low C-value, and the CVT secondary has a heavy inductive burden.

This section introduces logic that:

- Eliminates the distance element overreach due to CVT transients
- Causes minimum time delay for true in-zone faults
- Requires no special user settings
- Adapts to different SIRs

Before introducing this new CVT transient detection logic, we need to review some past solutions.

Past CVT Transient Overreach Solutions

Reach Reduction

One solution to CVT-transient-induced overreach is to reduce the Zone 1 reach. In some cases, the CVT transients could be so severe that Zone 1 protection must be eliminated (Figure 14).

Time Delay

Another method of avoiding Zone 1 distance relay overreach due to CVT transients is to introduce a fixed time delay for the Zone 1 elements. This time delay must be longer than the CVT transient duration.

The fixed time delay solution is a simple and effective way to solve the problem. However, the time delay is always present no matter what the SIR value is or where the fault is located. This time delay penalizes the fault clearing time even for a close-in fault on a low SIR system.

SIR Detection

Another solution is to detect the high SIR system condition using the measured voltage and current signals. When the voltage and current signals are below preset levels, the relay declares a high SIR condition. Once the high SIR condition is detected, additional filtering is introduced in the voltage channels, or a time delay is introduced in the distance element output decision. Both filtering and time delay methods have approximately the same effect.

The shortcomings with these SIR detection designs include the following:

- It is difficult to choose the overcurrent threshold setting. The setting is normally fixed by relay manufactures. If the setting is small, the relay has overreaching possibilities for some high SIR systems. If the overcurrent threshold setting is too large, the relay penalizes the fault clearing time for stronger systems.

- For high SIR systems, the fault currents for close-in and remote faults do not differ much. Relying only on the current level to detect high SIR conditions inevitably penalizes the tripping speed of close-in faults on high SIR systems.

Improved CVT Transient Detection Logic Description (Patent #5,703,745)

The following text describes the proposed CVT transient detection logic. Recall from Figure 14 that the distance element overreach increased with increasing SIR. The improved CVT detection logic uses this information to determine when time delay is necessary to eliminate the CVT transient effect. The major improvements of this logic include the following:

- The voltage and current thresholds are calculated automatically by the relay: no factory and user entered settings are required.
- Distance calculation smoothness is used to defeat the trip time delay for close-in faults on high SIR systems.

Figure 17 illustrates the block diagram of the CVT transient detection logic. The m is the distance calculation described in Reference [4] and δm is the incremental quantity of the distance calculation. In Figure 17, the 27 elements are phase-to-phase and phase-to-neutral undervoltage elements, and the 50 elements are phase-to-phase and phase-to-neutral overcurrent elements.

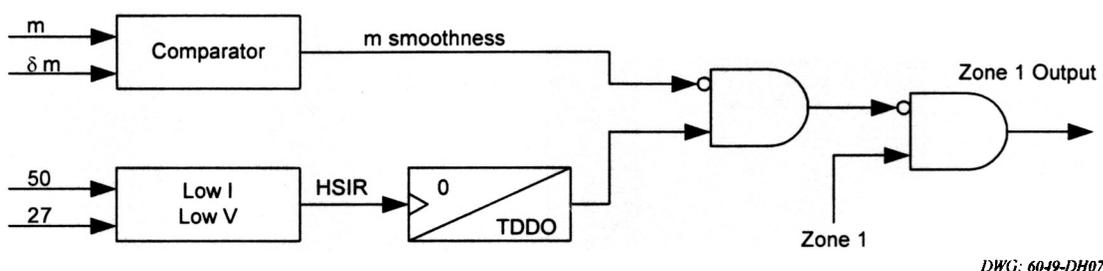


Figure 17 CVT Transient Detection Logic

Low-Voltage Detection

When the relay polarizing input voltage is depressed, we know that the relay voltage may include a CVT transient. We detect this low voltage with both phase-to-phase and phase-to-neutral undervoltage elements.

If an undervoltage element picks up and the corresponding overcurrent element does not, we identify this as a high SIR system condition. HSIR output in Figure 17 picks up. Upon detecting a high SIR condition, the CVT logic adds a short time delay (TDDO in Figure 17) to the Zone 1 elements to prevent distance element transient overreach. This delay is discussed later.

For phase-to-phase faults, it is the phase-to-phase voltage that decreases dramatically without an appreciable decrease in the phase-to-neutral voltage. Therefore, it is necessary to include separate phase-to-neutral and phase-to-phase undervoltage elements.

The CVT logic calculates the low-voltage thresholds based on a radial line with a predetermined SIR value. The threshold is the relaying voltage when a short circuit fault occurs at the end of the radial line. As shown in Figure 18, the CVT transient detection logic calculates the phase-to-neutral voltage threshold as followings:

$$V_{\text{phase}} = |V_0 + V_1 + V_2| = \frac{V_{\text{nom}}}{(\text{SIR} + 1)}$$

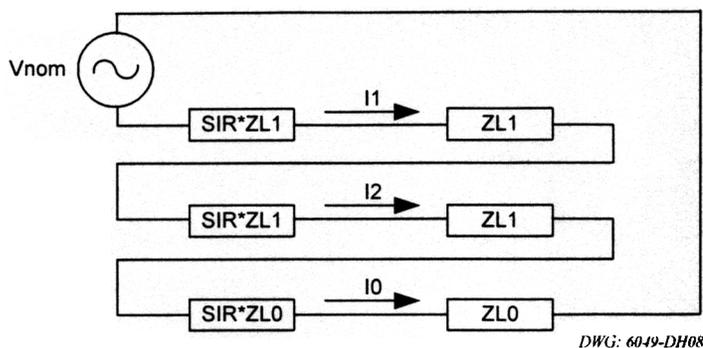


Figure 18 Sequence Network for an A-G Fault at Line End

As shown in Figure 19, the logic calculates the phase-to-phase voltage threshold as follows:

$$V_{\text{phase-phase}} = |(a^2 - a) \cdot (V_1 - V_2)| = \frac{\sqrt{3} \cdot V_{\text{nom}}}{(\text{SIR} + 1)}$$

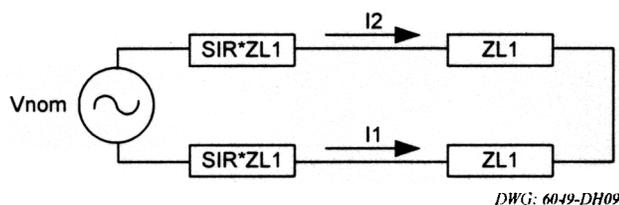


Figure 19 Sequence Network for a B-C Fault at Line End

High-Current Detection

A low-voltage condition by itself is insufficient to declare a high SIR system condition and thereby delays Zone 1 tripping because this condition is also present for close-in faults. To prevent Zone 1 tripping delay for a low SIR application and/or for close-in faults, we must supervise the low-voltage elements with corresponding high-current elements.

The CVT transient detection logic calculates the current thresholds using the user-entered replica line impedance settings and a predetermined SIR radial line model with the assumed fault location at the end of the line. The calculated current thresholds are the phase-to-neutral and phase-to-phase current flow at the relay.

Using the sequence network shown in Figure 18 as a reference, the logic calculates the phase-to-neutral current threshold as follows:

$$I_{\text{phase}} = |I_0 + I_1 + I_2| = \left| \frac{3 \cdot V_{\text{nom}}}{(\text{SIR} + 1) \cdot (2 \cdot Z_{L1} + Z_{L0})} \right|$$

Using the sequence network shown in Figure 19 as a reference, the logic calculates the phase-to-phase current threshold as follows:

$$I_{\text{phase-phase}} = \left| (a^2 - a) \cdot (I_1 - I_2) \right| = \left| 2 \cdot \sqrt{3} \cdot I_1 \right| = \left| \frac{\sqrt{3} \cdot V_{\text{nom}}}{(\text{SIR} + 1) \cdot Z_{L1}} \right|$$

The ratio of close-in to remote fault currents is (SIR + 1)/SIR. For a high SIR system, the fault current magnitudes do not differ greatly for different fault locations along the protected line section. Therefore, the high-current elements based on the thresholds calculated above do not override the undervoltage declaration for close-in faults on higher SIR systems. Thus, the distance element could be penalized with a delay for close-in faults. However, the logic we discuss next reduces this problem.

High SIR Time Delay and Distance Calculation Smoothness

As shown in Figure 17, with conditions of low voltage, low current, and the Zone 1 pickup, the CVT logic delays the Zone 1 element output. This delay is determined to be long enough to eliminate worst case CVT-transient-induced Zone 1 overreach.

For close-in faults on systems with high SIRs, we use the distance-calculation smoothness detection to override the tripping delay caused by low voltage and low current.

The high SIR detection (HSIR) part of the CVT logic could assert for close-in faults on higher SIR systems: low-voltage and low-current. This assertion is unavoidable on high SIR systems. However, there is a large difference in the distance calculation stabilization time for those cases with close-in faults and those cases with remote faults. In the later cases, the distance calculation stabilizes by the time the CVT transient dies out. In the former cases, the distance calculation stabilizes rather quickly, but the distance element operating speed is penalized by the CVT logic time delay. From these observations, we deduce that by detecting this “distance calculation smoothness,” we can bypass the time delay introduced by the CVT detection logic and thereby decrease tripping time. This logic then minimizes the fault clearing time delay of close-in faults on higher SIR systems where the CVT detection logic asserts due to low voltage and current.

The threshold of distance smoothness detection is a function of distance calculation results, which is experimentally determined as $-a \cdot m + b$. This variable threshold allows us to tolerate more distance calculation fluctuations when a fault is close-in and less if the fault is remote. This distance calculation-dependent threshold gives us the ability to override the CVT tripping delay for close-in faults occurring on high SIR systems.

CONCLUSIONS

- Faults occurring at voltage zero-crossings generate the worst-case CVT transient.
- The transients produced by CVTs with PFSC are much less than those produced by CVTs with AFSC.
- Distance element overreach due to CVT transients is not a problem for low SIR applications. This statement is true for CVTs with either AFSC or PFSCs.
- High-capacitance CVTs reduce distance element overreach because the transients they produce have a lower magnitude as compared to lower C-ratings for CVTs.

- Reducing the CVT burden also reduces distance element overreach. The resistive burdens found in microprocessor-based relays cause less CVT transients than the inductive burdens found in electromechanical relays.
- The proposed CVT transient detection logic is superior to past detection methods for the following reasons:
 - It does not require special user or factory settings.
 - It introduces minimum delay for in-zone faults.
 - It optimizes automatically the voltage and current thresholds for each application.
 - It uses m-smoothness calculations to bypass any unnecessary time delay for close-in faults.

REFERENCES

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3. ANSI C93.1-1990, For Power-Line Carrier Coupling Capacitors and Coupling Capacitor Voltage Transformers (CCVT) - Requirements, Section 5.1.10 Burdens.
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APPENDIX

This appendix shows circuits and the parameters of the active and passive CVTs that the paper uses in the CVT modeling. The appendix also lists the system and fault parameters that the paper uses in the Figure 11 modeling example.

ACTIVE CVT MODEL AND PARAMETERS

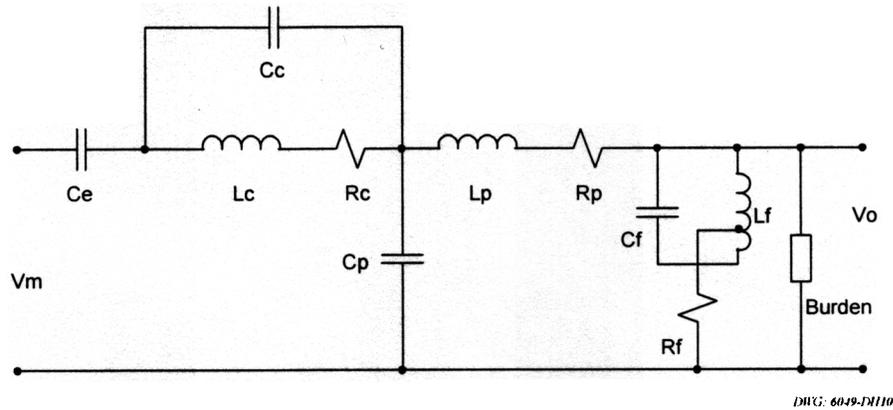


Figure 20 Active CVT Model

Where,	V_m	: intermediate voltage level,	5 kV
	C_e	: equivalent CVT capacitance (C_1+C_2),	100 nf
	C_c	: stray capacitance of the compensating inductor,	0.13 nf
	L_c	: inductance of the compensating inductor,	68 henry
	R_c	: copper resistance of the compensating inductor,	228 ohm
	C_p	: stray capacitance of the transformer,	0.14 nf
	L_p	: leakage inductance of the transformer,	2.8 henry
	R_p	: copper resistance of the transformer,	400 ohm
	C_f	: capacitance of the suppressing circuit,	9600 nf
	L_f	: inductance of the suppressing circuit,	0.7 henry
	R_f	: loading resistance of the suppressing circuit,	37.5 ohm
	mL_f	: middle tap of the suppressing inductor,	0.35

PASSIVE CVT MODEL AND PARAMETERS

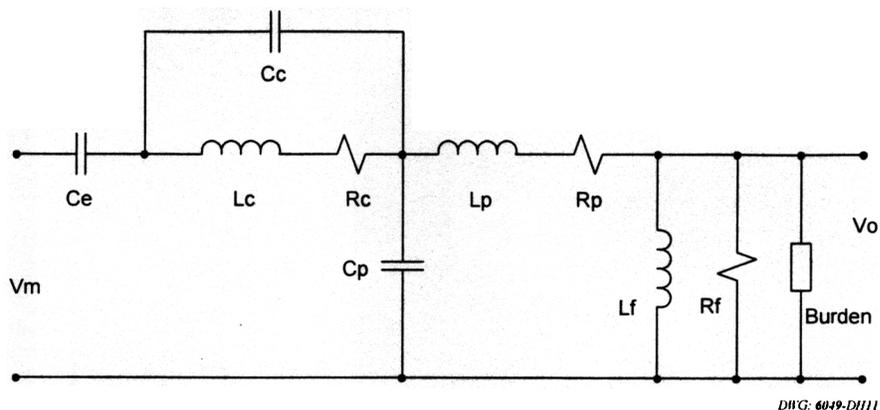


Figure 21 Passive CVT Model

Where,	V_m	: intermediate voltage level,	6 kV
	C_e	: equivalent CVT capacitance (C_1+C_2),	69.5 nf
	C_c	: stray capacitance of the compensating inductor,	1.16 nf
	L_c	: inductance of the compensating inductor,	101.2 henry
	R_c	: copper resistance of the compensating inductor,	127 ohm
	C_p	: stray capacitance of the transformer,	0.26 nf
	L_p	: leakage inductance of the transformer,	6.5 henry
	R_p	: copper resistance of the transformer,	296 ohm
	L_f	: inductance of the suppressing circuit,	16.5 henry
	R_f	: loading resistance of the suppressing circuit,	231 ohm

OTHER PARAMETERS

The radial system parameters:

Z_{sm}	: source impedance magnitude,	10 ohm
Z_{sa}	: source impedance angle,	87.5 degree
Z_{lm}	: line impedance magnitude,	1 ohm
Z_{la}	: line impedance angle,	87.5 degree

The fault parameters:

ϕ	: fault initiation angle,	270 degree
m	: fault location,	1.0 pu
r_f	: fault resistance,	0 ohm
r_{ld}	: load resistance,	200 ohm

CVT burden:

B_{cvt}	: resistive burden,	100 ohm
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BIOGRAPHY

Daqing Hou received BS and MS degrees in Electrical Engineering at the Northeast University, China, 1981 and 1984, respectively. He received his Ph.D. in Electrical and Computer Engineering at Washington State University in 1991. Since 1990, he has been with Schweitzer Engineering Laboratories, Inc., Pullman, Washington, USA, where he is currently a research engineer. His work includes system modeling, simulation and signal processing for power system digital protective relays. His research interests include multivariable linear systems, system identification, and signal processing. Hou is a member of IEEE. He has multiple patents pending and has authored or co-authored several technical papers.

Jeff Roberts received his BSEE from Washington State University in 1985. He worked for Pacific Gas and Electric Company as a Relay Protection Engineer for over three years. In 1988, he joined Schweitzer Engineering Laboratories, Inc. as an Application Engineer. He now serves as Research Engineering Manager. He has delivered papers at the Western Protective Relay Conference, Texas A & M University, Georgia Tech, and the South African Conference on Power System Protection. He holds multiple patents and has other patents pending. He is also a member of the IEEE.