



# SEL-3306 Synchrophasor Processor Guideform Specification

The SEL- 3306 Synchrophasor Processor shall operate as a synchronized phasor measurement data concentrator with network access to provide a combination of functions including, but not limited to, simultaneous collection of data from serial- and Ethernet-connected phasor measurement units (both SEL and non-SEL devices), correlation and concentration of collected data based on UTC time stamp, and simultaneous transmission of outgoing IEEE C37.118 protocol super packets and/or BPA PDC Stream synchrophasor data for as many as 6 client devices. The SEL- 3306 shall conform to various industry standards, operate in harsh environments, and provide the operational and functional requirements as described below:

**Power Supply.** The Synchrophasor Processor shall be capable of operating on a wide range of power supply voltages and shall be available with one of three power supply types: 85–300 Vdc or 85–264 Vac, 38–140 Vdc or 85–140 Vac, or 20–60 Vdc.

**Temperature.** The Synchrophasor Processor shall be capable of continuous operation over a temperature range of  $-40^{\circ}$  to  $+75^{\circ}\text{C}$  ( $-40^{\circ}$  to  $+167^{\circ}\text{F}$ ) to allow mounting in an outdoor control cubicle. The Synchrophasor Processor shall be type tested to IEC 60068-2-1:1990 (Test Ad 16 hr @  $-40^{\circ}\text{C}$ ), IEC 60068-2-2:1974 (Test Bd 16 hr @  $+75^{\circ}\text{C}$ ), and IEC 60068-2-30:1980 (Test Db 12 + 12-hour cycle @  $25^{\circ}$  to  $55^{\circ}\text{C}$ , 6 cycles).

**Environmental Testing.** The Synchrophasor Processor shall be tested to the same standards as protective relays. These standards shall include IEC 60255-21-1, IEC 60255-21-2, IEC 60255-21-3, IEC 60255-22-1, IEC 60255-22-2, EN61000-4-2, IEC 60255-22-3, IEC 60255-22-4, EN 61000-4-4, and IEEE C37.90.1 (see *Specifications* in the SEL-3306 Data Sheet for details).

**Communication Ports.** The Synchrophasor Processor shall have sixteen serial ports, and two Ethernet ports located on the rear panel. Two pins on serial ports one through fifteen shall be available for a demodulated IRIG-B time-synchronization signal. Ports one through fifteen shall have a selectable +5 Vdc output on Pin 1. The Console port shall be capable of operation at 9600 bps. Ports one through fifteen shall be capable of operation at 300–115200 bps. Ethernet ports shall be independent. All communication ports shall be ESD and RFI protected.

**Configuration.** The Synchrophasor Processor shall provide an EIA-232 serial port for initial configuration of the device. The Synchrophasor Processor shall provide terminal access to configure network settings.

**Alarm Output.** There shall be an alarm contact output to signal internal errors and malfunctions. The alarm contact shall be controlled by an internal watchdog system that independently monitors the operating system.

**Configuration Storage.** The Synchrophasor Processor shall store all configuration data in nonvolatile memory, allowing recovery after prolonged loss of power including failure of the internal battery.

**Moving Parts and Vent Holes.** The Synchrophasor Processor shall exclude all rotating disk drives, fans, moving parts, and vent holes.

**Warranty.** The Synchrophasor Processor shall be warranted for a minimum of 10 years.

